

Dual N-Channel 2.5-V (G-S) MOSFET

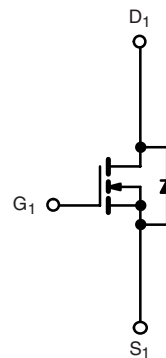
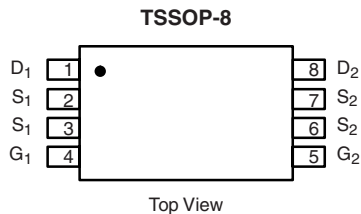
PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
20	0.030 at $V_{GS} = 4.5$ V	4.5
	0.033 at $V_{GS} = 3.0$ V	4.2
	0.035 at $V_{GS} = 2.5$ V	3.9
	0.043 at $V_{GS} = 1.8$ V	3.6

FEATURES

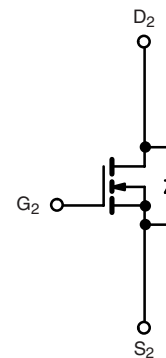
- Halogen-free



RoHS
COMPLIANT



N-Channel MOSFET



N-Channel MOSFET

Ordering Information: Si6926ADQ-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted					
Parameter	Symbol	10 s	Steady State	Unit	
Drain-Source Voltage	V_{DS}	20		V	
Gate-Source Voltage	V_{GS}	± 8		V	
Continuous Drain Current ($T_J = 150$ °C) ^a	I_D	$T_A = 25$ °C	4.5	4.1	A
		$T_A = 70$ °C	3.6	3.3	
Pulsed Drain Current (10 μ s Pulse Width)	I_{DM}	20		A	
Continuous Source Current (Diode Conduction) ^a	I_S	0.83	0.69	A	
Maximum Power Dissipation ^a	P_D	$T_A = 25$ °C	1.0	0.83	W
		$T_A = 70$ °C	0.64	0.53	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150		°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ s	90	125	°C/W
		Steady State	126	150	
Maximum Junction-to-Foot (Drain)	R_{thJF}	65	80	°C/W	

Notes:

a. Surface Mounted on FR4 board, $t \leq 10$ s.

For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>.

* Pb containing terminations are not RoHS compliant, exemptions may apply.

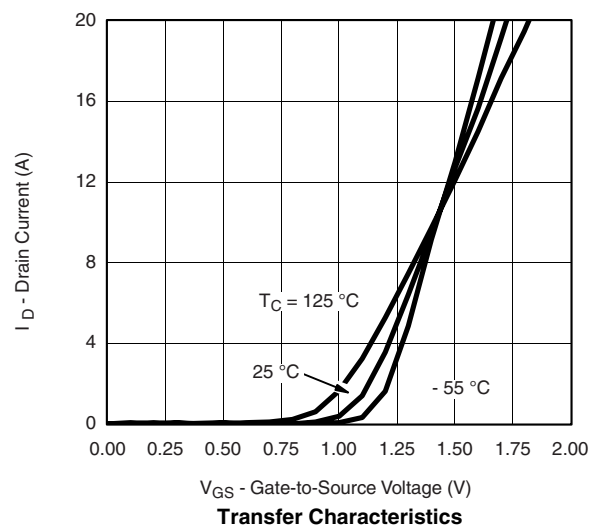
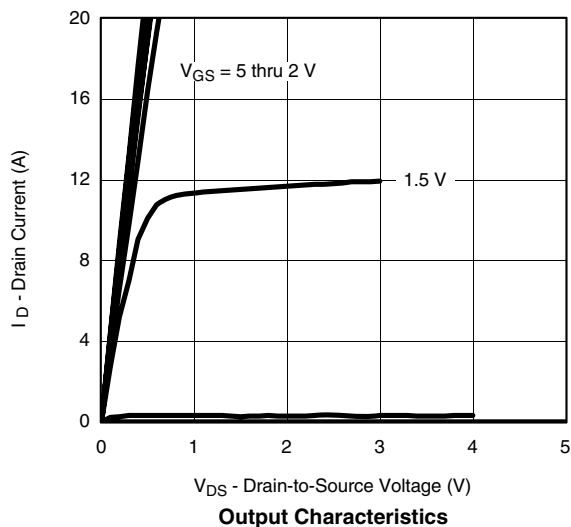
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.40		1.0	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			5	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 5\text{ V}$	10			A
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 4.5\text{ A}$		0.024	0.030	Ω
		$V_{GS} = 3.0\text{ V}, I_D = 4.2\text{ A}$		0.026	0.033	
		$V_{GS} = 2.5\text{ V}, I_D = 3.9\text{ A}$		0.029	0.035	
		$V_{GS} = 1.8\text{ V}, I_D = 3.6\text{ A}$		0.035	0.043	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 4.5\text{ A}$		26		S
Diode Forward Voltage ^b	V_{SD}	$I_S = 0.83\text{ A}, V_{GS} = 0\text{ V}$		0.6	1.1	V
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 4.5\text{ A}$		7.5	10.5	nC
Gate-Source Charge	Q_{gs}			1.2		
Gate-Drain Charge	Q_{gd}			1.2		
Gate Resistance	R_g			1.9		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 10\text{ }\Omega$ $I_D \cong 1\text{ A}, V_{GEN} = 10\text{ V}, R_g = 6\text{ }\Omega$		6	12	ns
Rise Time	t_r			16	25	
Turn-Off Delay Time	$t_{d(off)}$			46	70	
Fall Time	t_f			9	15	
Source-Drain Reverse Recovery Time	t_{rr}		$I_F = 0.83\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		20	

Notes:

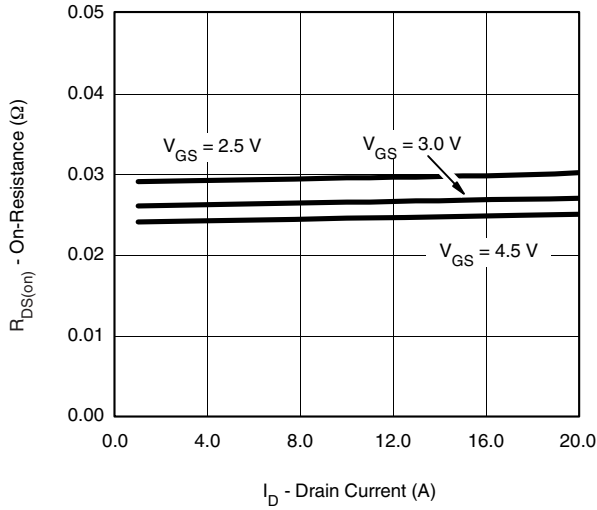
- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

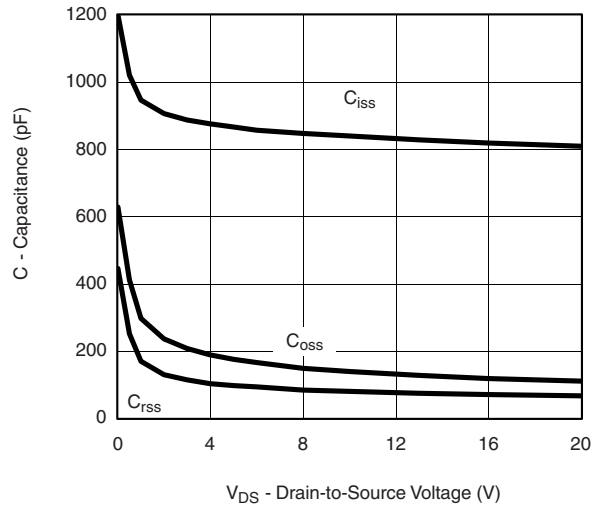
TYPICAL CHARACTERISTICS $25\text{ }^\circ\text{C}$, unless otherwise noted



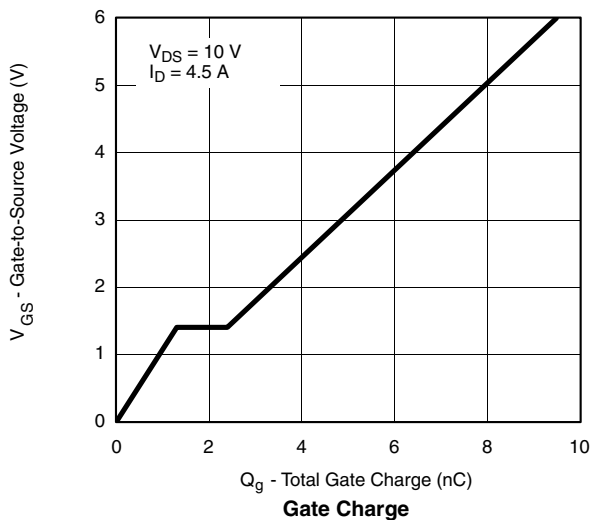
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



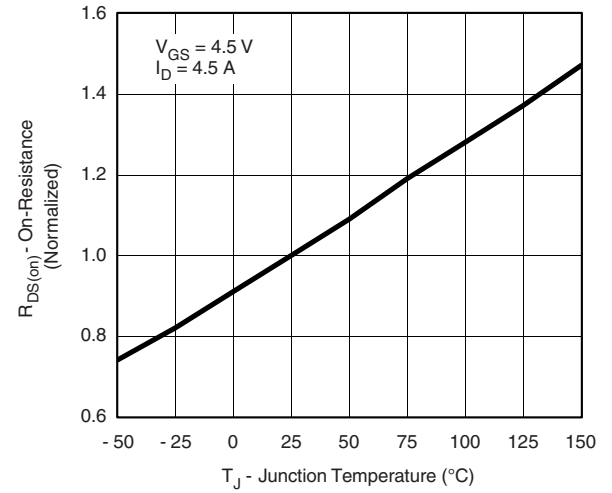
On-Resistance vs. Drain Current



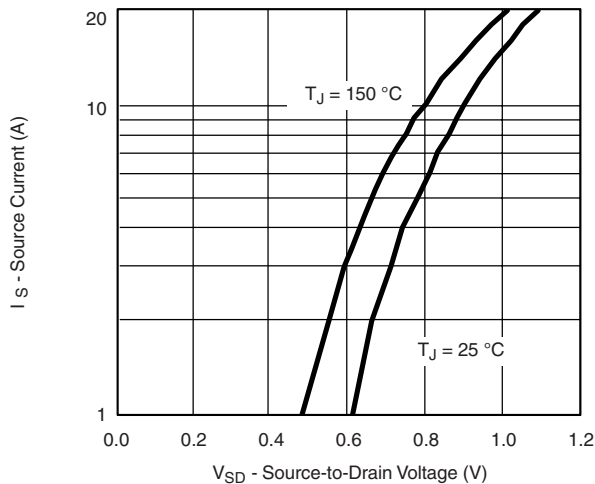
Capacitance



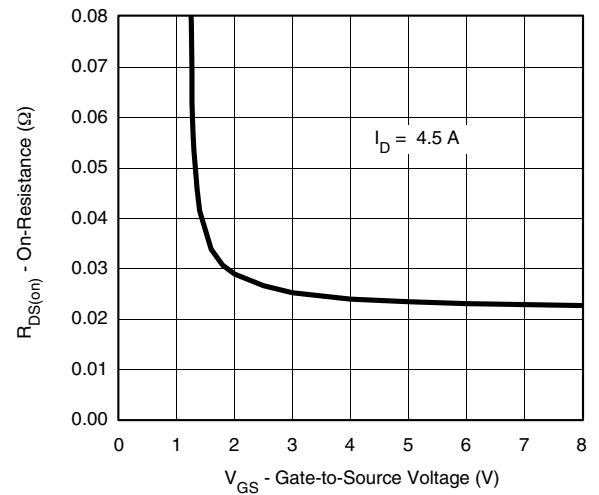
Gate Charge



On-Resistance vs. Junction Temperature

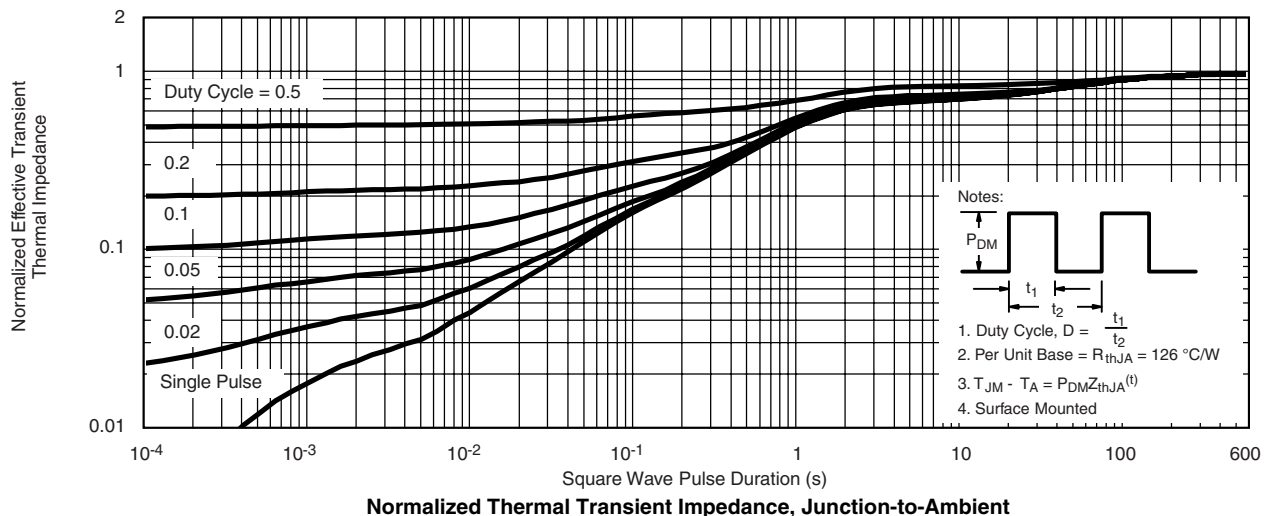
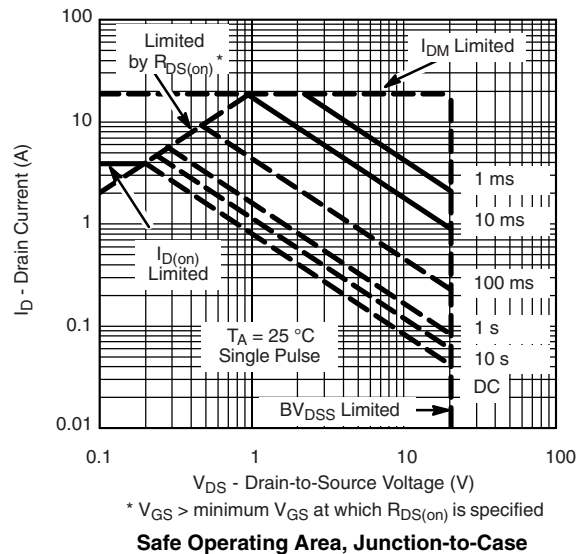
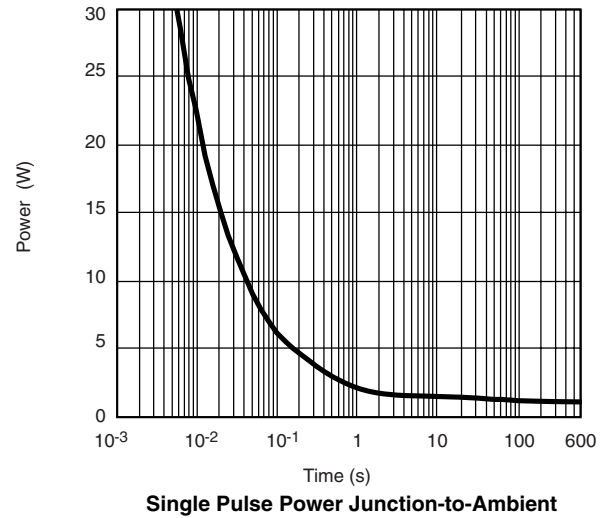
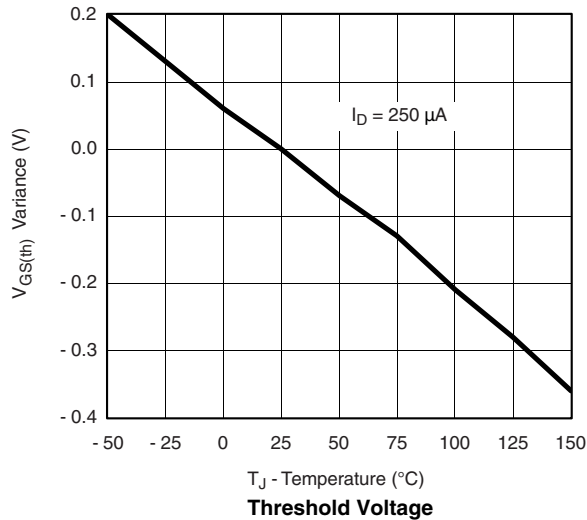


Source-Drain Diode Forward Voltage



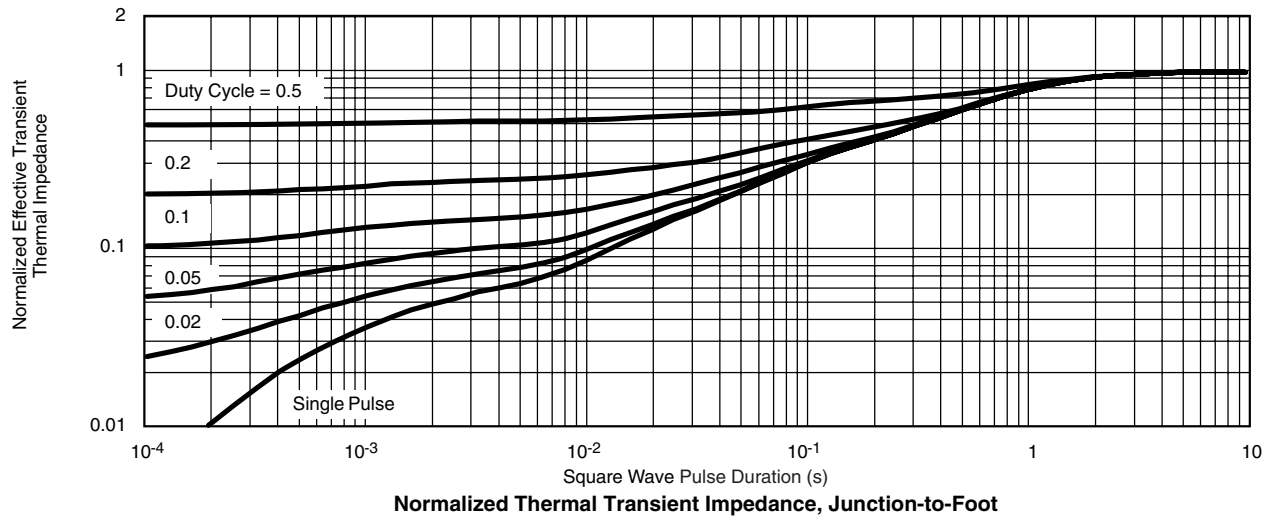
On-Resistance vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?72754>.



Disclaimer

All product specifications and data are subject to change without notice.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained herein or in any other disclosure relating to any product.

Vishay disclaims any and all liability arising out of the use or application of any product described herein or of any information provided herein to the maximum extent permitted by law. The product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein, which apply to these products.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications unless otherwise expressly indicated. Customers using or selling Vishay products not expressly indicated for use in such applications do so entirely at their own risk and agree to fully indemnify Vishay for any damages arising or resulting from such use or sale. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

Product names and markings noted herein may be trademarks of their respective owners.